普 誠 科 技
Princeton Technology Corp.

DESCRIPTION

The RX3310A is a fully integrated, amplitude-shift-keying (ASK) modulation, single chip receiver. It is designed to operate in a variety of low power radio applications. All popular radio frequencies from 250 MHz to 450 MHz may be supported by simply choosing the appropriate external components. Particular emphasis has been placed on low current consumption.
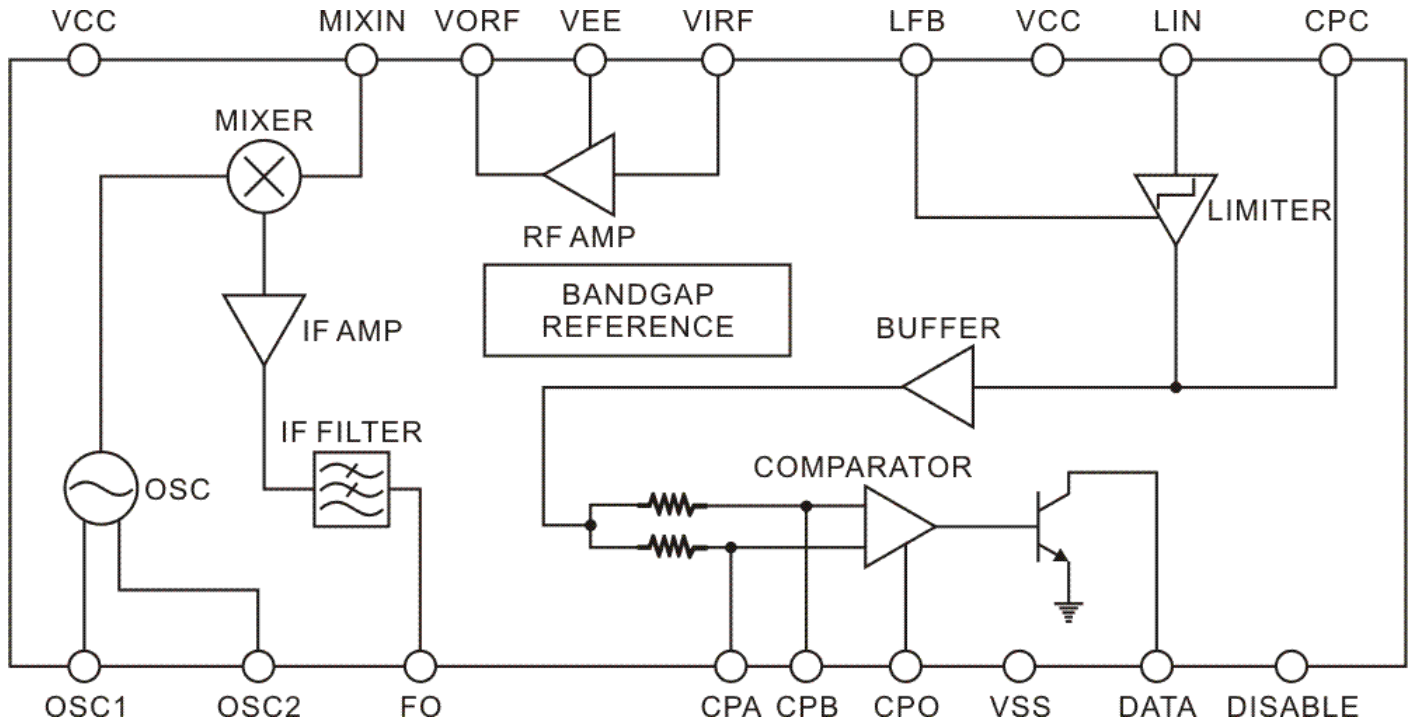
FEATURES

- Wide frequency range: 250 MHz to 450 MHz
- High sensitivity
- Low power consumption
- High integration level
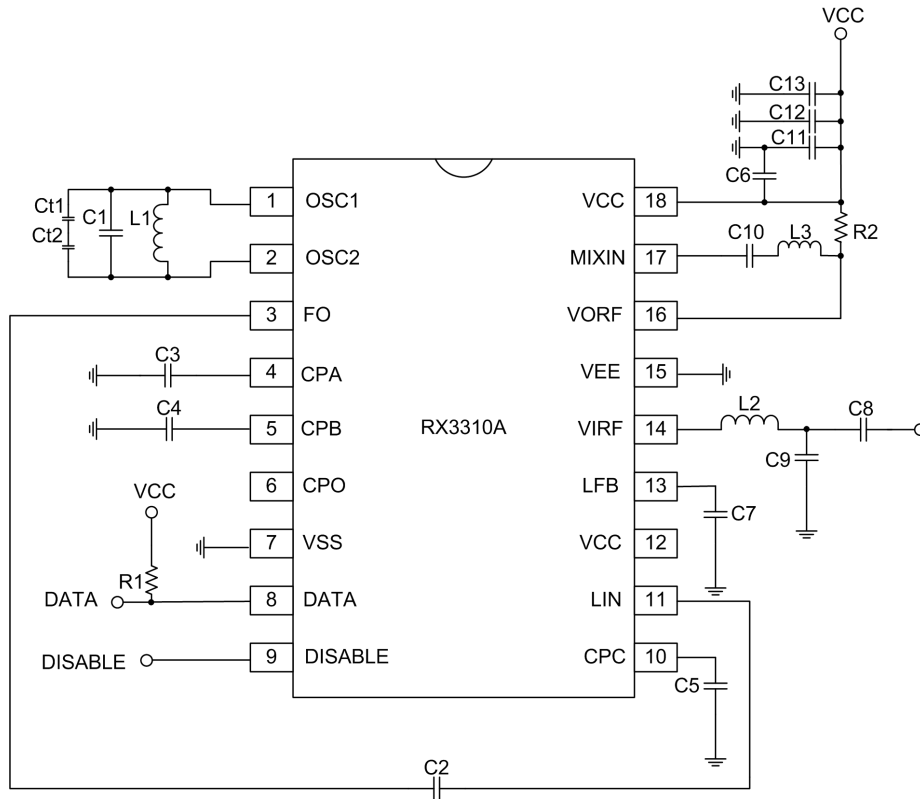- SOP 18L package or SSOP 20L (150 mil) package

APPLICATIONS

- Remote control systems
- Car alarm and other security systems
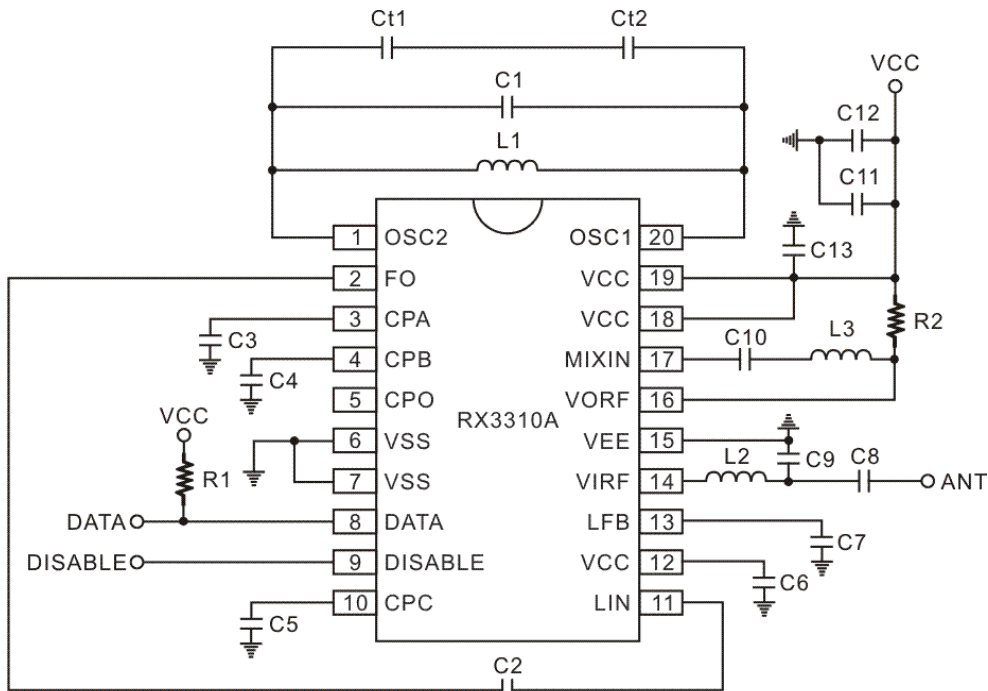- Baby finder, wireless doorbell, wireless toys

BLOCK DIAGRAM

APPLICATION CIRCUIT

18 PINS, SOP

20 PINS, SSOP

Note: Ct1, Ct2 are added for the temperature compensation. Not necessary.

EXTERNAL COMPONENTS

Component	Frequency Band (MHz)		Unit	Tolerance	Remark
	315	434			
C1	8.2	6.8	pF	±0.5pF	TC = NPO
C2	100	100	pF	±5%	TC = NPO
C3	560	560	pF	±10%	TC = X7R
C4	1	1	µF	±10%	TC = Y5V
C5	1	1	nF	±10%	TC = X7R
C6	10	10	nF	±10%	TC = X7R
C7	10	10	nF	±10%	TC =X7R
C8	100	100	pF	±0.25pF	TC = NPO
C9	4.7	8.2	pF	±0.25pF	TC = NPO
C10	100	120	pF	±5%	TC = NPO
C11	10	10	nF	±10%	TC = X7R
C12	3.3	3.3	µF	±10%	TC = Y5V
C13	470	470	pF	±10%	TC = X7R
Ct1					
Ct2					
R1	100	100	KΩ	±5%	TC = ±200 ppm
R2	680	680	Ω	±5%	TC = ±200 ppm
L1	2.5	1.5	T		tunable
L2	100	56	nH		
L3	100	68	nH		

Note: All components are SMD 0603 type.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
RX3310A	18 Pins, SOP, 300mil	HiMARK RX3310A-LF
RX3310A	20 Pins, SSOP, 150mil	HiMARK RX3310A-LF

PIN CONFIGURATION

18 PINS, SOP

```
OSC1   [ 1        18 ]  VCC
OSC2   [ 2        17 ]  MIXIN
FO     [ 3        16 ]  VORF
CPA    [ 4        15 ]  VEE
CPB    [ 5   HiMARK  14 ]  VIRF
CPO    [ 6  RX3310A-LF  13 ]  LFB
VSS    [ 7        12 ]  VCC
DATA   [ 8        11 ]  LIN
DISABLE[ 9        10 ]  CPC
```

20 PNS, SSOP

```
OSC2   [ 1        20 ]  OSC1
FO     [ 2        19 ]  VCC
CPA    [ 3        18 ]  VCC
CPB    [ 4        17 ]  MIXIN
CPO    [ 5   HiMARK  16 ]  VORF
VSS    [ 6  RX3310A-LF  15 ]  VEE
VSS    [ 7        14 ]  VIRF
DATA   [ 8        13 ]  LFB
DISABLE[ 9        12 ]  VCC
CPC    [ 10       11 ]  LIN
```
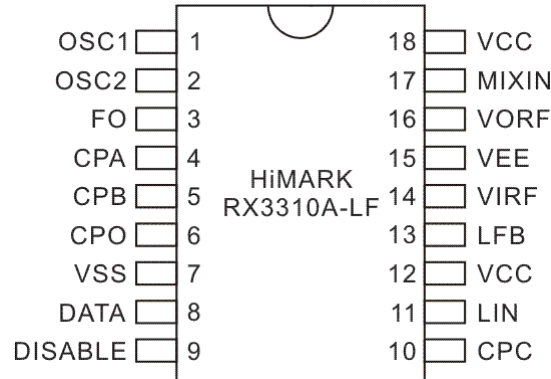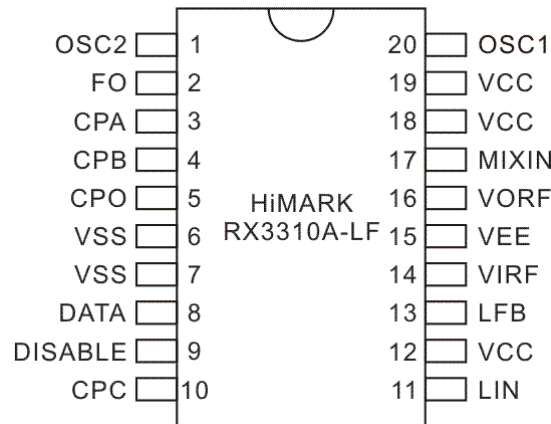
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			18-pin SOP	**20-pin SSOP**
OSC1	IO	Oscillator tank connection	1	20
OSC2	IO	Oscillator tank connection	2	1
FO	O	IF filter output	3	2
CPA	I	Comparator input A	4	3
CPB	I	Comparator input B	5	4
CPO	I	Comparator offset adjustment	6	5
VSS	GND	Ground	7	6, 7
DATA	O	Data output	8	8
DISABLE	I	Disable input. See Electrical Characteristics (V_{CC} = 5.0 V) on page 6	9	9
CPC	I	Comparator input C	10	10
LIN	I	Limiter input	11	11
VCC	POWER	Positive supply voltage	12	12
LFB	IO	Limiter feedback B	13	13
VIRF	I	RF amplifier input (requires external ac decoupling capacitor)	14	14
VEE	GND	Ground for RF amplifier	15	15
VORF	O	RF amplifier output	16	16
MIXIN	I	Mixer input (requires external ac decoupling capacitor)	17	17
VCC	POWER	Positive supply voltage	18	18, 19

FUNCTION DESCRIPTION

RF AMPLIFIER

The RF amplifier uses a common emitter configuration with a separate emitter connection (VEE). The input signal (VIRF) should be ac-coupled externally. The output of the amplifier is open collector so that the gain may be set with an external tuned load.

MIXER

The mixer is doubly-balanced configuration and has an ac-coupled input.

OSCILLATOR

A balanced oscillator configuration is used with an L-C tank externally connected across the OSC1 and OSC2 pins. The frequency of the oscillator is determined by the external capacitor, C1, and inductor, L1 (please refer to application circuit schematic).

IF AMPLIFIER

The IF amplifier is a differential input, single-ended output emitter-coupled pair. It is used to provide additional gain in order to reduce the influence of the noise of the succeeding limiter amplifier on the total receiver noise figure.

IF FILTER

To minimize external component costs, an active IF filter is fully integrated.

LIMITER

The limiting amplifier consists of several dc-coupled amplifier stages and outputs an RSSI signal.

COMPARATOR

Following the limiting amplifier, the RSSI signal is passed through an additional buffer stage and is then fed to the comparator's positive and negative terminals, which possess different R-C filter time constants. A larger off-chip capacitor is used at the negative comparator input and hence, its terminal voltage represents the average value of the RSSI signal. A smaller off-chip capacitor is used at the positive comparator input and this allows the positive input to follow the RSSI signal instantaneously. When the received RSSI signal exceeds its average value (when an ASK on signal is received), the comparator output is switched on.

BAND GAP REFERENCE

A band gap reference provides precise biasing of the entire chip over temperature.

ABSOLUTE MAXIMUN RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	V_{SS}-0.3 to V_{SS}+6.0	V
Operating temperature range	Topr	-20 to +60	℃
Storage temperature range	Tstg	-60 to +125	℃
Soldering temperature range	T_{SLD}	255	℃
Soldering time range	t_{SLD}	10	s

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage range	V_{CC}	2.4	3.0	6.0	V
Operating temperature	T_A	-20	-	60	℃

RECEIVER CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 3.0 V, V_{SS} = 0 V, LO-RF = 1.8 MHz, All test at T_A = 25℃)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Sensitivity	P_{sens}	V_{CC} = 3.0 V, T_A = 27℃, AM99%, sine wave (ASK square wave)	-100 (-104)	-98 (-102)		dBm
Maximum input power	$P_{in,max}$			-35	-30	dBm
Receiver turn-on time	t_{ON}				5	ms

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 3.0 V, V_{SS} = 0 V, All test at T_A = 25℃)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply current	I_{CC}			3	4.5	mA
Standby current	$I_{CC,sb}$	DISABLE = high		5	10	µA
Disable pin input logic high[Note1]	V_{DIH}		2.3	3.0		V
Disable pin input logic low[Note1]	V_{DIL}				0.8	V
Data output logic high	V_{OH}		V_{PP}[Note2]-0.3V			V
Data output logic low	V_{OL}				0.3	V

(Unless otherwise specified, V_{CC} = 5.0 V, V_{SS} = 0 V, All test at T_A = 25℃)

| Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply current	I_{CC}			4.5	5.0	mA
Standby current	$I_{CC,sb}$	DISABLE=high		5	10	µA
Disable pin input logic high[Note1]	V_{DIH}		4.3	5.0		V
Disable pin input logic low[Note1]	V_{DIL}				0.8	V
Data output logic high	V_{OH}		V_{PP}[Note2]-0.3V			V
Data output logic low	V_{OL}				0.3	V

Notes:
1. If the Disable pad is connected to an off-chip signal (open), then the pad is internally grounded.
2. V_{PP} is the pull-up voltage for open collector data output.

EVALUATION BOARD LAYOUT (EXAMPLE)

20 PINS, SSOP
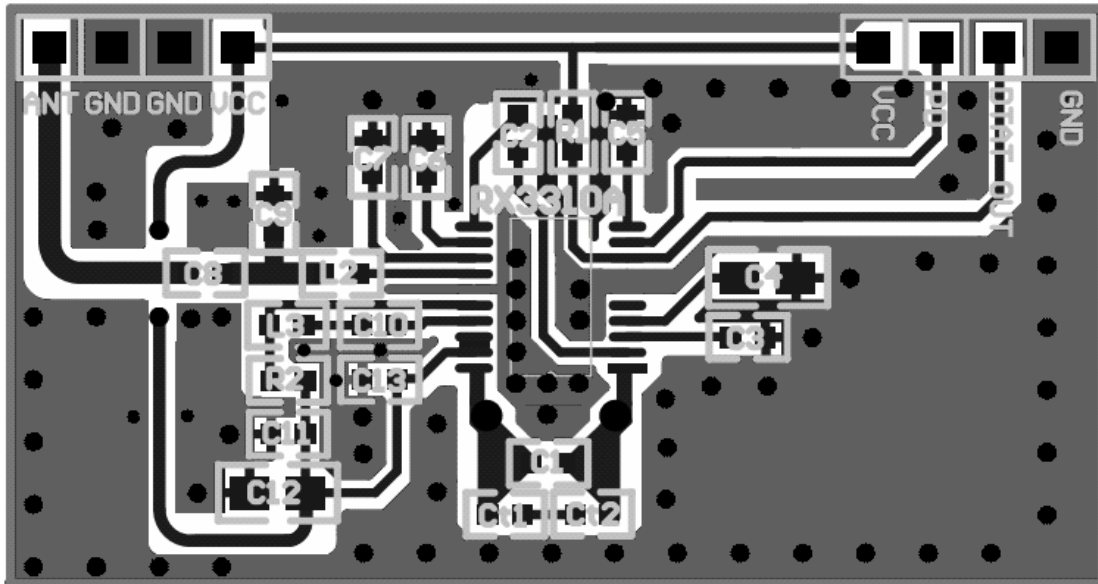

RX3310A PCB Top Layout
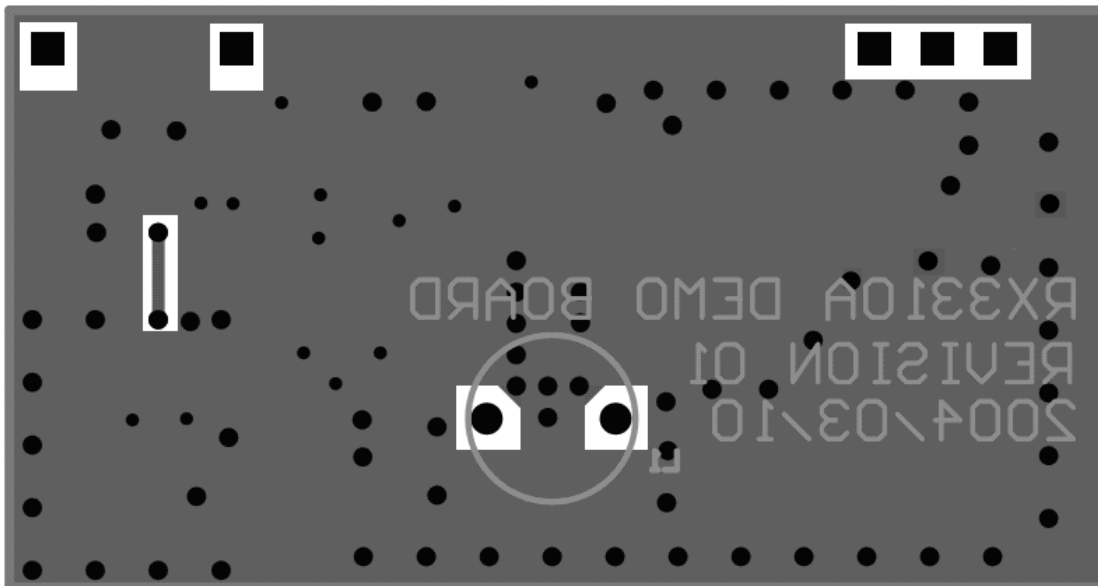
RX3310A PCB Bottom Layout

Notes:
1. From top to bottom: Component side of printed-circuit board, top side, bottom side.
2. The PCB portal file is available. The real size printed-circuit board is available. (Real-size: 1753 mil x 934 mil)
3. Suggested board material: FR4, thickness: 1.0 mm

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PACKAGE INFORMATION

18 PINS, SOP, 300MIL
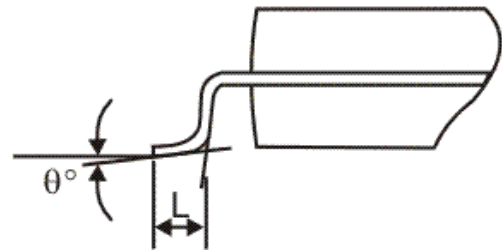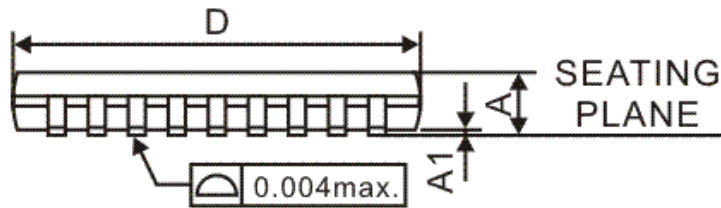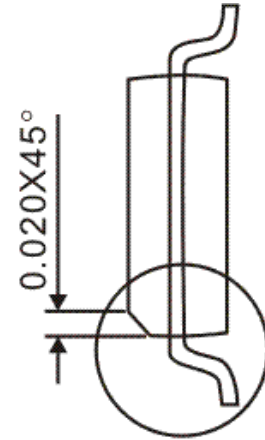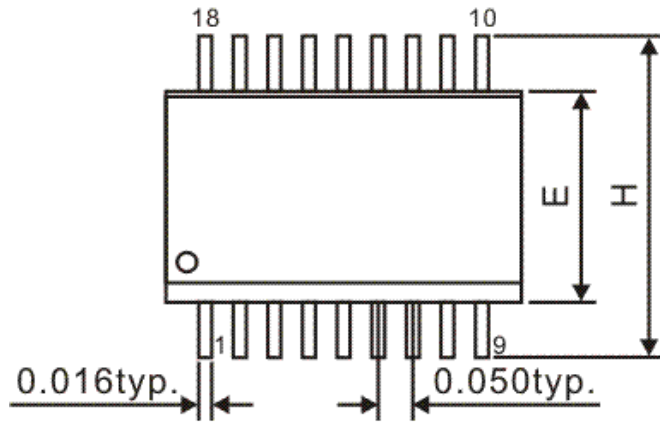
Symbol	Min.	Max.
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ	0°	8°

Notes:

1. Controlling dimension is Inch.
2. JEDEC outline: MS-013 AB.
3. Dimensions "D" does not include mold flash, protrusions or gate burrs, mold flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
4. Dimensions "E" does not include inter-lead flash, or protrusions. Inter-leas flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.

20 PINS, SSOP, 150MIL
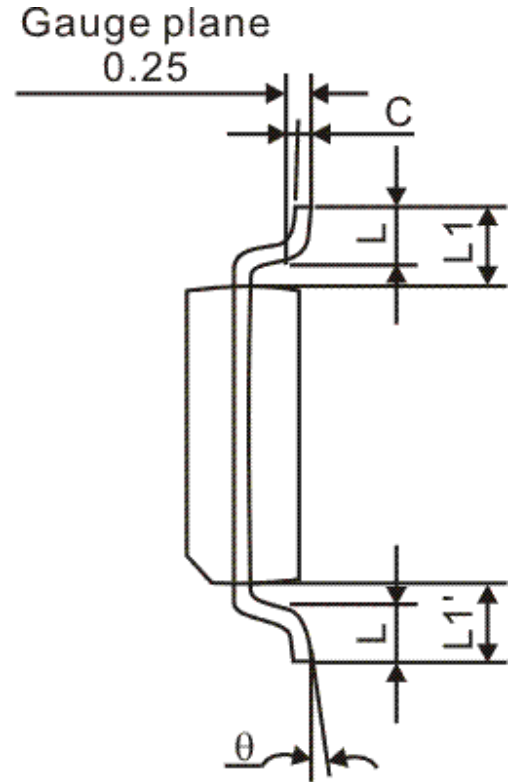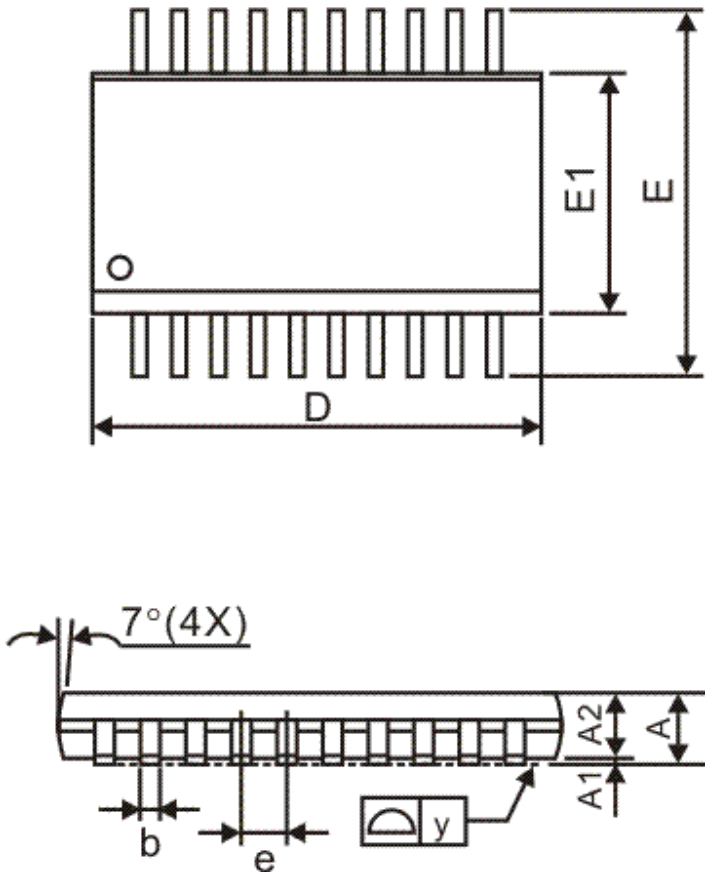
Symbol	Min.	Nom.	Max.
A	1.35	1.60	1.75
A1	0.10	-	0.25
A2	-	1.45	-
b	0.20	0.25	0.30
C	0.19	-	0.25
D	8.55	-	8.75
E	5.80	6.0	6.20
E1	3.80	3.9	4.00
e	-	0.64	-
L	0.40	-	1.27
y	-	-	0.10
θ	0°	-	8°
｜L-L1'｜	-	-	0.12
L1	1.04 REF.		

Notes:
1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gage plane.
3. Tolerance 0.10 mm unless otherwise specified.
4. Controlling dimensions are in millimeter. Converted inch dimensions are not necessarily exact.
5. Followed from JEDEC MO-137.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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REVISION HISTORY

Date	Revision No.	Reference No.	Modification
1/16/2009	RX3310A V2.0	Request no.: 090106 Approval no.: 090115	1. new format 2. modify Features 3. p2, replace Application circuit 4. p5, delete chip window 5. p7, Absolute Maximum Rating, Operating temperature range -40~+85 ➜ -20~+60 6. p7, Recommended Operating Conditions, Supply voltage range min. ➜ 2.4 p7, Recommended Operating Conditions, Operating temperature -40~+85 ➜ -20~+60 7. p7, Electrical Characteristics (V_{CC}=3.0V), Disable pin input logic high min. ➜ 2.3V; Type ➜ 3.0V p7, Electrical Characteristics (V_{CC}=5.0V), Disable pin input logic high min. ➜ 4.3V; Type ➜ 5.0V 8. p7, Receiver Characteristic condition: V_{CC}=2.0V to 6.0V ➜ Vcc = 3.0V, Vss=0V 9. p8, Evaluation Board Layout, delete 18-pin SOP layout; replace 20-pin SSOP layout figures.